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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,753	11/17/2003	Leonard Forbes	400.260US01	3377

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,753	FORBES, LEONARD	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-11 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5, 7-11, 23 are pending.

The remarks and amendments made on 08/18/2006 are fully considered but found not persuasive. Applicant argues that a separate oxide layer is formed above each source/drain region. As shown in Fig. 2 and paragraph 0026, the oxide materials 211 and 210 are present on two different areas (source and drain). It doesn't mean that the oxide layers on source and drain regions are two different layers. The oxide layer formed on source and drain regions could be the same layer but since it is formed on two different areas, it can be called as the first layer and the second layer. The oxide layers 211 and 210 in Fig. 2 could be the same layer.

Portion of layer 18 in Eitan structure which present on the source region could be called as the first oxide layer, and portion of the layer 18 which present the drain region could be called as the second oxide layer. Fig. 2 of Eitan reads over the limitations cited in amended independent claims 1, 9, and 23. In addition, Fig. 1C of Ling (U.S. Patent No. 5,811,852) also discloses the first oxide layer formed on the source region and the second oxide layer formed on the drain region.

Claims 1-5, 7-11, 23 are still rejected.

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-11, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan, U.S. Patent No. 6,552,387, in view of Ling, U.S. Patent No. 5,811,852.

Regarding claims 1, 9, and 23, See Figs. 2-3, 18B, and Cols. 1-28, Eitan discloses a planar NROM transistor or a processor that generates control signals for the system, a memory array coupled to the processor and having a plurality of memory cells (Col. 1; EEPROM) comprising a substrate layer 12 (or 62) having two source/drain regions 14/16 (or 58/60) separated by normally fully depleted body region (the channel, and the heavily doped channel shown in Eitan, lines 55-57, Col.2, is inherently a fully depleted channel), a first and second oxide layers (portions of layer 18 on source and drain regions) formed above each of the source/drain regions (parts of source/drain regions are beneath the layer 18 (or layer 56); Figs. 2-3), a gate insulator 20 (or 54)

formed over the body region and oxide layer, the gate insulator capable of storing a plurality of charges in different locations of the insulator (reverse and forward directions; Figs. 2-3); and a control gate 24 (or 50) formed on the gate insulator. Eitan fails to disclose the substrate is an ultra thin silicon on insulator layer. Ling discloses the structure of EEPROM whereas the substrate is the silicon on insulator layer. Ling also discloses a first oxide layer formed on the source region and a second oxide layer formed on the drain region (Fig. 1C). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a silicon-on-insulator layer as a substrate in the method of forming ROM because the silicon on insulator layer is used to improve the performance of transistors, exhibits low resistance, the thickness, impurity concentration, and crystalline perfection can be controllable.

Still regarding claim 9, Eitan fails to disclose a substrate comprises an insulator layer and the silicon on insulator layer and wherein the thickness of the silicon on insulator layer is less than 100 nm. However, the selection of such parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed

"critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Regarding claims 7-8, It is inherent that the transistor of EEPROM in Eitan has NAND and NOR architectures.

Regarding claims 2-5, it is conventional that the gate insulator is an ONO, oxide-nitride-aluminum oxide, or one of silicon oxides formed by wet oxidation or not annealed, silicon rich oxides composite structures because these composite structures are well known to be the best structures that capable of trapping charges.

Regarding claim 10, Eitan discloses the control gate is comprises of a polysiicon material.

Regarding claim 11, Eitan discloses wherein the first source/drain regions operates as a drain region when the cell is operated in the first direction and as a source region when the cell is operated in the second direction (reverse and forward directions).

Eitan, "NROM: A Novel Localized Trapping, 2-bit Nonvolatile memory Cell" (submitted as IDS on 05/26/2004), also discloses the same invention as cited in claims 1, 9, and 23.

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

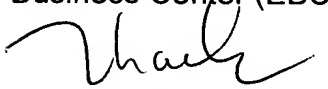
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1785. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. Other inquiries of this application should be called to (571) 272-1562 or the fax number (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le
Primary Examiner
Art Unit 2818
September 8, 2006.